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INVESTIGATION OF HOMOEPITAXIAL Si GROWTH DEPOSITED BY ELECTRON BOMBARDMENT ONTO THE Si (100) SUBSTRATE

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Abstract

We have investigated the deposition condition of thin epitaxial Si layers onto the Si (100) substrates by electron bombardment (EB) evaporation and the recrystallization condition of the deposited Si layer aiming at the formation of the patterned SOI substrate. In this study, Si layers were first deposited on the Si (100) substrates for 500, 1000, 2000 s at room temperature (RT) for the calibration of deposition rate. The thicknesses of the deposited Si layers were measured by the Rutherford backscattering spectrometry. Next, we have deposited Si layers on the chemically cleaned Si (100) substrates at RT to investigate the epitaxial growth conditions. The samples were then annealed at 800□ and 1000□ for 10−180 min in the ultrahigh vacuum (UHV) environment. The crystallinity of the deposited Si layer was evaluated by reflection high energy electron diffraction method and the surface morphology was observed by the atomic force microscope. As a result, the deposited Si layers have been found to be recrystallized three-dimensionally after the samples were annealed in the UHV environment.

I. Introduction

Si-on-insulator (SOI) structure consists of a surface crystalline Si (SOI) layer separated from a substrate by a buried oxide (BOX) layer. This structure has excellent electric properties of high-speed performance, low-energy consumption and high-radiation hardness compared to those of the bulk Si structure.

We aim at forming patterned SOI substrates in the future that are composed of both SOI (SOI/BOX thicknesses of 10−20 nm) and bulk regions (as shown in Fig. 1). This structure is expected as high-speed and power-saving random-access-memory by forming trench-capacitor circuits on the bulk region and access-transistor circuits on the SOI region [1, 2]. However, it is difficult to form these hybrid structures, using a wafer-bonding SOI-formation method. Therefore, we have investigated Si homoepitaxial growth on the patterned SiO_2 structure synthesized on the Si substrate by electron bombardment (EB) evaporation of Si. Subsequently, we recrystallize laterally the evaporated Si amorphous layer on the SiO_2 by furnace annealing or by high-energy ion-beam-irradiation annealing method [3, 4] (Fig. 2).

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In this study, we exanimated the optimum conditions of the Si deposition by EB evaporation and the recrystallization of the evaporated amorphous Si on the crystalline Si (100) substrate.

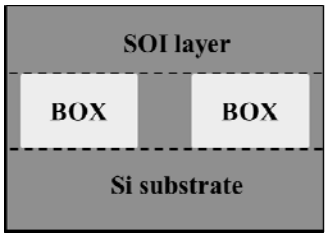

Fig. 1. Schematic image of patterned SOI substrate.

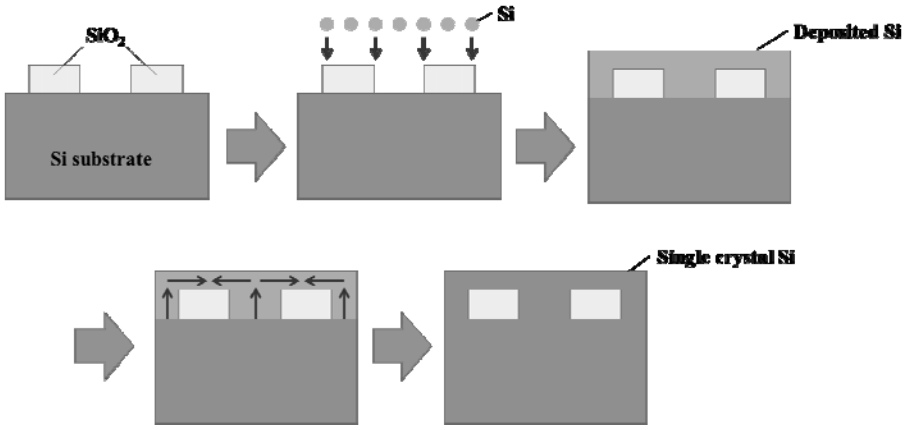

Fig. 2. Formation method of patterned SOI structure by EB evaporation.

II. Experiment

In this study, amorphous Si layers were firstly deposited on the crystalline Si (100) substrates using an EB evaporator in the ultrahigh vacuum (UHV) environment at room temperature (RT) for 500-2000 s. The film thickness of the deposited amorphous Si layer was measured by the Rutherford backscattering spectrometry (RBS). We then estimated the optimum deposition condition to form uniform Si layers with several-tens-nm thick. Secondly, we prepared the chemically-cleaned Si (100) substrates and deposited Si layers with approximately 20 nm thick. The samples were annealed at 800 and 1000 □ for 10－180 minutes in the UHV environment for recrystallization of the deposited amorphous Si layer. Finally, the crystallinity of the annealed Si layers was evaluated by the RHEED and the surface morphology of the samples was observed by the AFM.

III. Results and discussion

Figure 3 shows the estimated film thickness of the as-deposited Si layers analyzed by the RBS. The film thickness increased linearly with deposition time. We obtained the deposition rate of 0.7 nm/min. However, from the RBS spectra, the deposited Si layer contained some impurities distributed throughout the entire depth of the deposited film (see Fig. 4). The impurity peaks were observed in the channels higher than those of Si for the sample of every deposition period. The impurity and the substrate peaks were best-fitted when we assumed the impurity element with the mass number of around 40. In addition, oxygen was observed uniformly in the deposited layer.

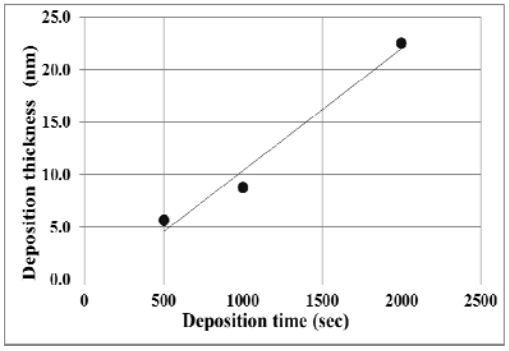

Fig. 3. Estimated deposition rate.

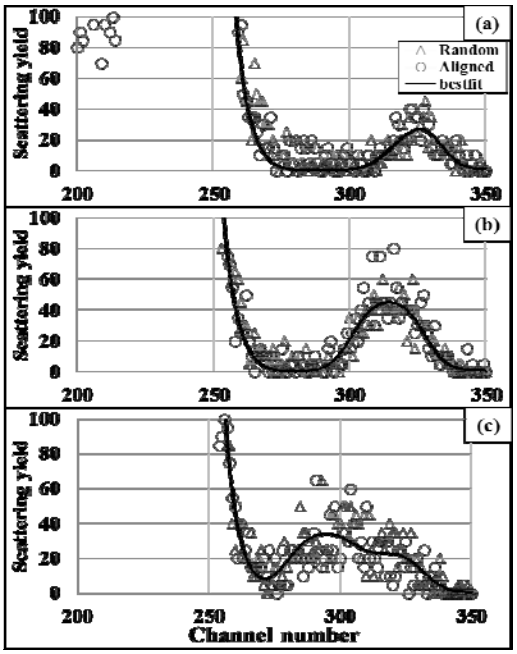

Fig. 4. RBS spectra of impurities observed in the deposited Si layer.
Deposition periods are (a) 500, (b) 1000 and (c) 2000 s, respectively.

Figure 5 shows RHEED patterns indicating the crystallinity of these three samples. Fig. 5 (a) shows the pattern for the chemically-cleaned Si (100) surface, corresponding to the diffraction pattern of the crystalline Si (100) surface. Figs. 5(b) and (c) show the annealed-samples in which Si layers were deposited in advance with 20 nm thick. In those figures, we observed diffraction patterns of the single crystal Si. However, transmission diffraction spots were confirmed in Fig. 5(b) and (c). The appearance of the transmission diffraction pattern means that the sample surfaces are not flat. The surface morphology of these annealed-samples are shown in Figs. 6(a) and 6(b), using the AFM. Figs. 6(a) and (b) show the minute surface morphology of the annealed-samples, corresponding to those shown in Figs. 5(b) and (c), respectively. From the profiles of both samples, the island sizes were approximately estimated to be 40 nm high, 160 nm wide for the 800□-annealed sample (Fig. 6(a)), and approximately 40 nm high, 180 nm wide for the 1000□-annealed sample (Fig. 6(b)).

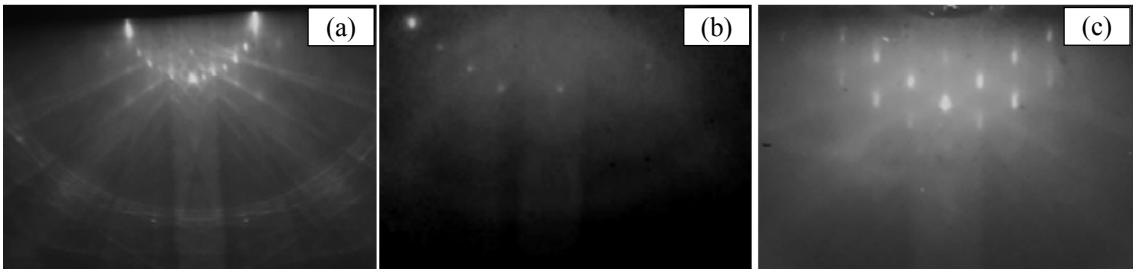

Fig. 5. RHEED patterns of (a) chemically cleaned Si (100) substrate, (b) post-annealed at 800□ for180 min, and (c) post-annealed at 1000□ for 10 min.

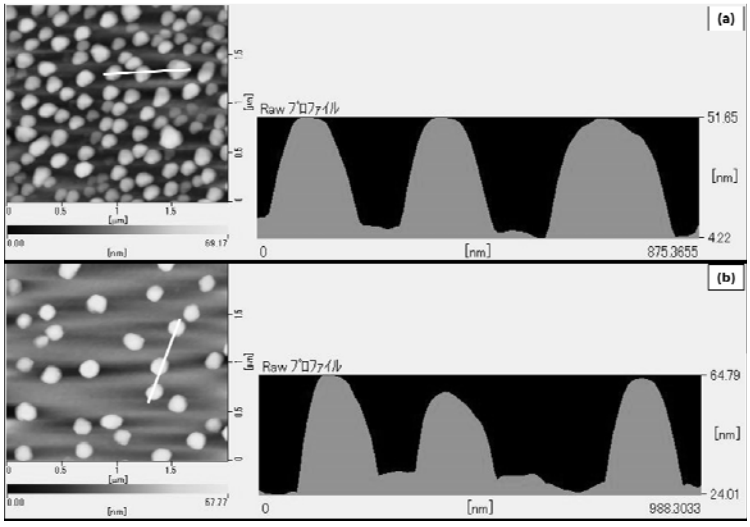

Fig. 6. Surface morphology observed by AFM
[(a) post-annealed 800□ for 180 min, (b) post-annealed 1000□ for 10 min]

IV. Conclusions

In this study, we exanimated the optimum conditions of epitaxial Si growth on the Si (100) substrate by the EB evaporation. As a result, we confirmed that the deposited Si layer was recrystallized but formed three-dimensional island structures when the samples were post-annealed at 800 and 1000□ in UHV environment. In addition, some impurities were detected in the deposited Si layer.

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