

CURRENT CROWDING CAUSED BY SURFACE ROUGHNESS OF VERTICAL GaN p-n DIODES

Hayashi, Kentarou / Mishima, Tomoyoshi / Nakamura, Tohru
/ Ohta, Hiroshi

(出版者 / Publisher)

法政大学イオンビーム工学研究所

(雑誌名 / Journal or Publication Title)

PROCEEDINGS OF THE 35th SYMPOSIUM ON MATERIALS SCIENCE AND ENGINEERING
RESEARCH CENTER OF ION BEAM TECHNOLOGY HOSEI UNIVERSITY (December 7,
2016)

(巻 / Volume)

35

(開始ページ / Start Page)

53

(終了ページ / End Page)

57

(発行年 / Year)

2017-02

(URL)

<https://doi.org/10.15002/00030378>

CURRENT CROWDING CAUSED BY SURFACE ROUGHNESS OF VERTICAL GaN p-n DIODES

Kentarou Hayashi*, Hiroshi Ohta, Tohru Nakamura and Tomoyoshi Mishima
*Department of Electrical and Electronics Engineering, Hosei University, Koganei,
Tokyo 1840003, Japan*

This paper presents EL intensity mapping on a p-n junction plane of vertical GaN diodes under forward biased conditions for the first time. By this mapping, it has been discovered that current crowding has existed corresponding to naturally formed surface stripes on epitaxial layers grown on freestanding GaN substrates. Detailed analyses by AFM and TOF-SIMS clarified that concentration of doped Mg acceptors on one slope of the stripe was higher than that on the other slope. The higher Mg-concentration region should have lower electric resistances, which would cause the current crowding. By improving the surface flatness, the current crowding was suppressed and a low specific on-resistance was obtained.

I. Introduction

Gallium Nitride (GaN) has excellent physical properties compared with those of the commonly used Si, such as a wide band gap, a high breakdown electric field, a high saturation-drift velocity, and a high thermal conductivity. By these properties, great attentions have been paid for GaN in applications to highly efficient power devices. GaN p-n junction diodes with high breakdown voltages (VB) have been reported by several researchers [1]-[5]. In a recent paper, the record VB of 4.7 kV combined with a low specific differential on-resistance (Ron) of $1.7 \text{ m}\Omega\text{cm}^2$ was achieved [5]. Crystal growth and device-fabrication technologies of GaN devices are not as matured as those of Si and SiC; hence in-depth investigations are still required. GaN fortunately is a direct energy-band gap semiconductor and strong electroluminescence (EL) occurs by recombination of electrons and holes under forward-biased conditions, which leads considerable reduction of Ron [6]-[7]. The EL intensity is proportional to injected current; therefore, microscopic EL mapping can give information on local current distributions in the p-n junction plane. In this study, we have succeeded to obtain clear EL images by introducing a transparent cathode electrode. We found anomalous EL images with striped patterns which corresponded to surface morphologies of the GaN p-n junction epitaxial wafers. Improvement of current-voltage characteristics have been obtained with a smooth featureless wafer.

II. Experimental

The detailed schematic structure of the p-n diode is shown in Fig.1. The layer structure was grown by metal-organic vapor-phase epitaxy (MOVPE) on a free-standing GaN substrate fabricated by the void-assisted separation (VAS) method with threading dislocation densities less than $3 \times 10^6 \text{ cm}^{-2}$ [8]-[9]. Electron density, mobility, diameter and thickness of the used substrate were $1.5 \times 10^{18} \text{ cm}^{-3}$, $40 \text{ cm}^2/\text{Vs}$, 2 inch and 0.4 mm, respectively. Trimethylgallium (TMG), ammonia (NH_3), bicyclopentadienyl-

* Corresponding author: e-mail kentaro.hayashi.3r@stu.hosei.ac.jp

magnesium (Cp_2Mg), and silane (SiH_4) were used as precursors. Drift layers under the p-GaN layer consisted of n⁻-GaN with a Si concentration of $1 \times 10^{15} \text{ cm}^{-3}$ and n⁻-GaN with a Si concentration of $8 \times 10^{15} \text{ cm}^{-3}$. A smooth surface wafer and a naturally stripe-patterned wafer with the same layer structure were prepared.

For device processing, a mesa dry etching was performed which was followed by a deposition of Pd/Ni (200 nm/100 nm) circular electrode with a diameter of 200 μm on exposed p⁺-GaN as an ohmic contact, and field plate (FP) metal electrode of Ti/Al (30 nm/250 nm) was deposited on the ohmic metal. The FP structure has been proved to be effective in the electric field relaxation [1]. Finally, Indium-Tin-Oxide (ITO) (500 nm) was deposited on the rear face of the GaN substrate to form a transparent cathode electrode for evaluation of the EL emission intensity in the p-n junction region directly. After deposition of the ITO, post thermal annealing was carried out at 500 ° C for 30 minutes under an air atmosphere in order to increase the transmittance by compensating for oxygen vacancies. Current-voltage (I-V) characteristics were evaluated using Agilent B1505A combined with an ultra-high-voltage unit at room temperature. The EL mapping was performed from the backside of the diodes by Horiba's LabRAM HR system. An atomic force microscope (AFM) was used for the evacuations on the surface roughness and Time-of-Fright Secondary Ion Mass Spectrometry (TOF-SIMS) for impurity-distribution mapping of the wafer.

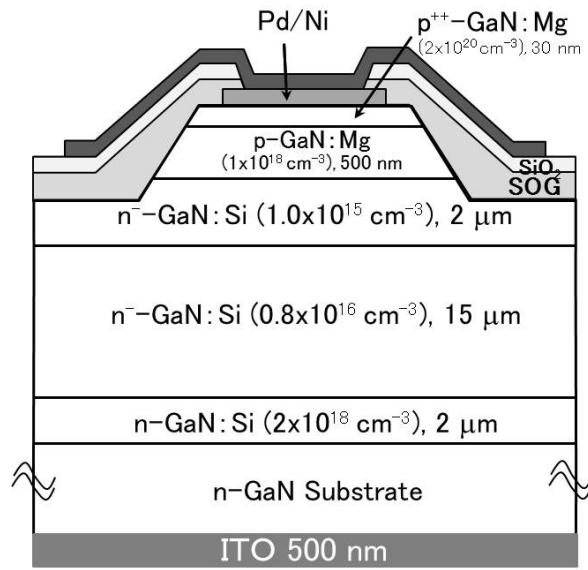


Fig.1. Schematic cross section of the GaN p-n junction diode with the FP structure.

III. Results and Discussions

Figure 2 shows the AFM image of the GaN wafer with the striped surface morphology. Repeated V-shaped stripes were observed. Along the diagonal line with a length of 100 μm in the figure, the height distribution by cross-sectional AFM image is shown in Fig. 3. The difference in height between peak and valley was about 70 nm. A convex area was formed by slopes with different angles of inclination. The gentle slope had larger roughness than that of the sharp slope by observation of detailed AFM images (not shown in the figure).

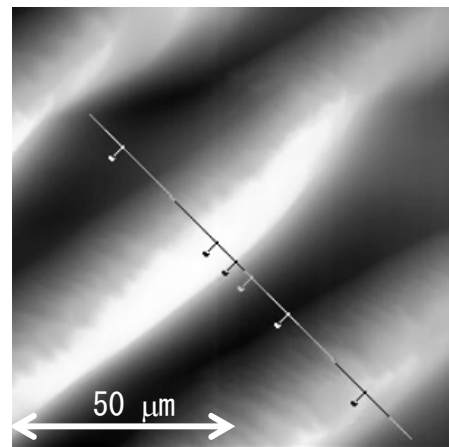


Fig.2. AFM image of the GaN wafer with the striped surface morphology.

Figure 4 is an optical microscopic image of the fabricated p-n junction diode with the Pd anode electrode of 400 μm in diameter. The striped surface morphology was observed. Figure 5 shows the microscopic EL mapping image of the same diode under forward biased conditions. The EL image showed corresponding pattern to the image in Fig.4. By careful

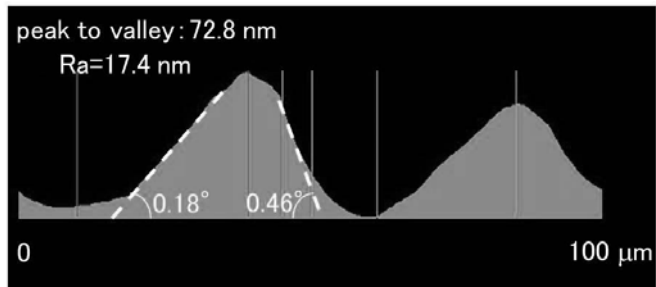


Fig.3. Cross-sectional AFM image of the GaN wafer with the striped surface morphology.

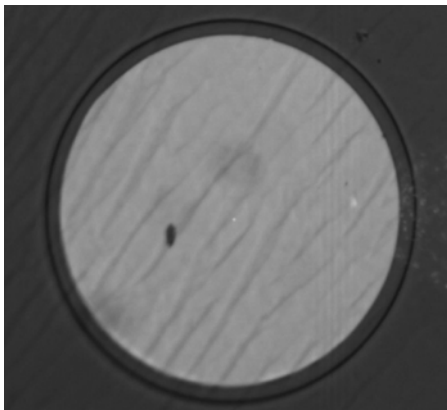


Fig.4. Optical microscopic image of the GaN wafer with Pd electrode of 400 μm in diameter.

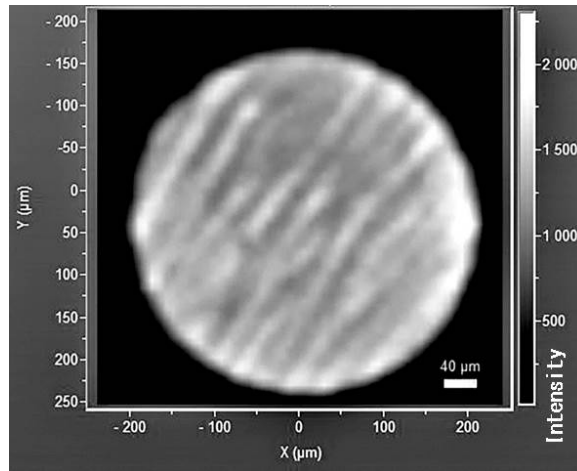


Fig.5. Microscopic EL mapping image of the diode under forward biased conditions.

comparison, it was found that the gentle slopes exhibited higher EL intensity. Impurity mapping image was taken by TOF-SIMS in order to clarify the cause of the inhomogeneous EL emission. Figure 6 shows the mapping image of Mg distribution. It was found that the Mg concentration was higher in the gentle slope than that of the sharp slope. It is conceivable that capture efficiency of Mg during the MOVPE growth would be higher on the gentle slope with the larger roughness which generated more atomic steps on the surface.

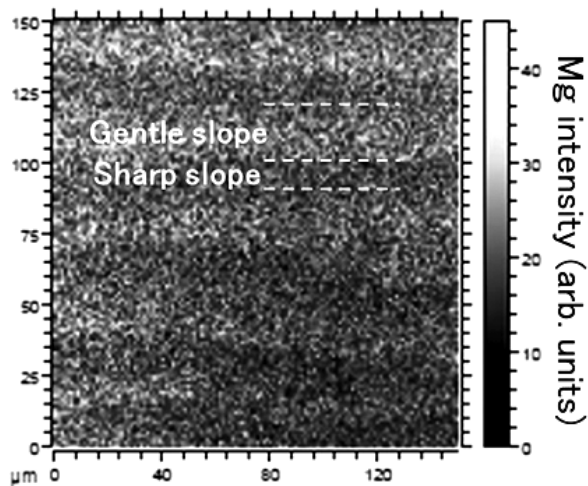


Fig.6. Plan-view Mg distribution of GaN p-n diode wafer by TOF-SIMS (150 x 150 μm^2).

I-V characteristics of the diodes with smooth (peak-to-valley height < 20 nm) and striped (peak-to-valley

height > 50 nm) surfaces are shown in Fig. 7. The current characteristics in the logarithmic scale did not differ much by the roughness. The ideality factors of the diodes were between 1 and 2 at the current range < 10 A/cm² which suggested the absence of leakage current. But at the high current region > 100 A/cm², the diodes with the smooth surface showed lower *Ron* than those with the striped surface. Figure 8 shows a summary of *Ron* of the diodes fabricated in this study. Apparently the diodes with the smooth surface had low *Ron*'s with a small deviation of < 2 %. The deviation for the striped surface diodes was about 7 %.

These results suggested that precisely controlled epitaxial layers in surface quality would be essential for fabricating high performance GaN p-n junction diodes.

IV. Conclusions

EL intensity mapping on a p-n junction plane of vertical GaN power diodes under forward biased conditions has been successfully observed by introducing transparent cathode electrodes for the first time. Existence of the current crowding was found with corresponding patterns of naturally formed surface stripes on epitaxial layers grown on freestanding GaN substrates. The higher current density regions were located on the one-side gentle slopes of the stripes, where higher density Mg acceptors were detected by TOF-SIMS analysis. The diodes with smooth surfaces showed low *Ron*.

Acknowledgement

The authors thank the Japan Ministry of the Environment for giving us the opportunity of this sturdy.

References

[1] Y. Hatakeyama, K. Nomoto, A. Terano, N. Kaneda, T. Tsuchiya, T. Mishima, and T. Nakamura, "High-Breakdown-Voltage and Low-Specific-on-Resistance GaN p-n

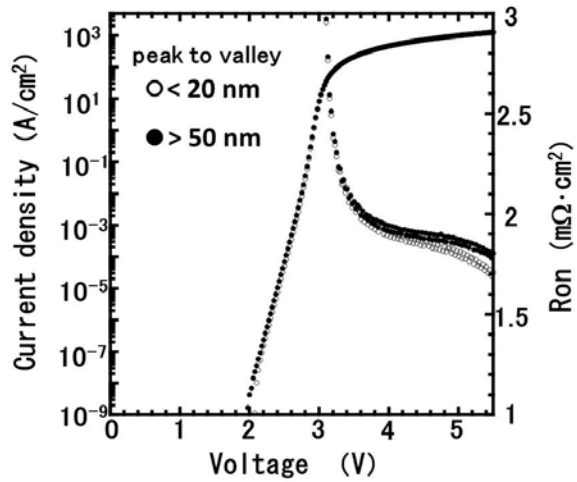


Fig.7. I-V characteristics of the GaN p-n diodes with the different roughness.

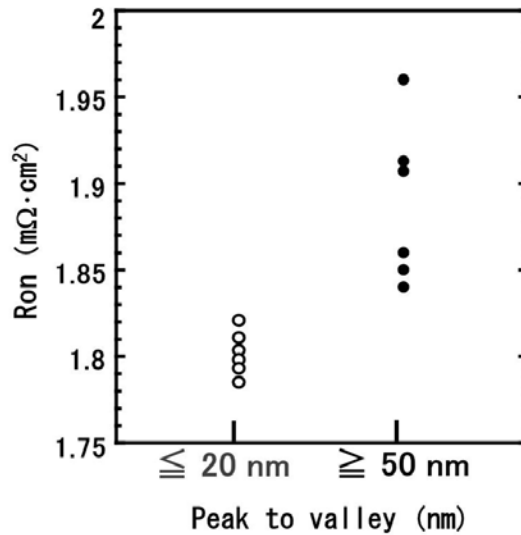


Fig.8. *Ron* dependence on the roughness.

Junction Diodes on Free-Standing GaN Substrates Fabricated Through Low-Damage Field-Plate Process," *Jpn. J. Appl. Phys* **52**, 028007-1-3 (2013).

- [2] H. Ohta, N. Kaneda, F. Horikiri, Y. Narita, T. Yoshida, T. Mishima, and T. Nakamura, "Vertical GaN p-n junction diodes with high breakdown voltages over 4 kV," *IEEE Electron Device Letter* **36**, 11, 1180-1182 (2015).
- [3] I. C. Kizilyalli, T. Prunty, and O. Aktas, "Avalanche Capability of Vertical GaN p-n Junctions on Bulk GaN Substrates," *IEEE Electron Devices Letters* **36**, 10, 1073-1075 (2015).
- [4] K. Nomoto, Y. Hatakeyama, H. Katayose, N. Kaneda, T. Mishima, and T. Nakamura, "Over 1.0 kV GaN p-n junction diodes on free-standing GaN substrates," *Phys. Stat. Sol. (A)* **208**, 7, 1535-1537, Jul. (2011).
- [5] Y. Hatakeyama, K. Nomoto, N. Kaneda, T. Mishima, and T. Nakamura, "Over 3.0 GW/cm² figure-of-merit GaN p-n junction diodes on free-standing GaN substrates," *IEEE Electron Device Lett* **32**, 12, 1674-1676, Dec. (2011).
- [6] K. Mochizuki, T. Mishima, K. Nomoto, A. Terano, and T. Nakamura, "Optical-thermo-transition model of reduction in on-resistance of small GaN p-n diodes" *Jpn. J. Appl. Phys* **52**, 08JN10-1-4, May (2013).
- [7] K. Mochizuki, T. Mishima, Y. Ishida, Y. Hatakeyama, K. Nomoto, N. Kaneda, T. Tshuchiya, A. Terano, T. Tsuchiya, H. Uchiyama, S. Tanaka, and T. Nakamura, "Determination of lateral extension of extrinsic photon recycling in p-GaN by using transmission-line-model patterns formed with GaN p-n junction epitaxial layers" *Jpn. J. Appl. Phys* **52**, 08JN22 -1-4, May (2013).
- [8] Y. Oshima, T. Eri, M. Shibata, H. Sunakawa, K. Kobayashi, T. Ichihashi, and A. Usui, "Preparation of freestanding GaN wafers by hydride vapour phase epitaxy with void-assisted separation," *Jpn. J. Appl. Phys* **42**, 1A/B, L1-L3, Jan. (2003).
- [9] T. Yoshida, Y. Oshima, T. Eri, K. Ikeda, S. Yamamoto, K. Watanabe, M. Shibata, and T. Mishima, "Fabrication of 3-in GaN substrates by hydride vapour phase epitaxy using void-assisted separation method," *J. Cryst. Growth* **310**, 1, 5-7, Jan. (2008).