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NORMALLY-OFF OPERATION OF ION IMPLANTED MISFET USING FREESTANDING GaN SUBSTRATES

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ABSTRACT. This paper describes DC characteristics of ion implanted MISFET on freestanding GaN substrates. When V_d = 10 V, V_{th} obtained from extrapolation of linear portion of transconductance was 9 V. These excellent normally off characteristics are brought by the low defect density GaN epitaxial layers and our optimized ion-implantation process which minimize the additional defect formation during the high temperature annealing.

I.Introduction

Gallium nitride (GaN) is an ideally suitable material for applications in high power, high frequency, and high temperature devices due to its remarkable properties such as a wide bandgap, a high breakdown electric field, a high saturation velocity, and high thermal conductivity [1]. One of the applications of GaN is AlGaN/GaN HEMT, which has been much focused by many researchers as it can be successfully applied to high frequency, high power devices [2-3]. HEMTs are well known as normally-on operation which is a disadvantage for the switching devices with high voltage. Normally-off operation is required to avoid multiple power supply and circuit complexity. Several investigations on the normally-off AlGaN/GaN HEMTs have been performed by a recessed gate and N-face substrates [4-5]. However, these measures still have challenges in complexity of processes and current collapse. Recently, normally-off GaN MISFETs have been reported; however their threshold voltages (V_{th}) were less than 4 V or their drain current (I_d) was not sufficiently suppressed at their claiming V_{th} [6-8]. This paper describes an increase in V_{th} of GaN MISFET fabricated using a p-GaN layer grown on the high quality freestanding GaN substrates.

II. Device Fabrication

A schematic cross section of device structure of an ion implanted GaN MISFET is shown in Fig. 1. The layer structures were grown by MOVPE on sapphire and n-GaN substrates with a low threading dislocation density of 10^6 cm^{-2}. The p-GaN layer was doped with Mg at concentrations of 5×10^{17} or 1×10^{18} cm^{-3}. A 30 nm thick SiN_x dielectric film was deposited by sputtering method. Si ions were implanted at a dose of 1×10^{15} cm^{-2} at an energy of 50 keV to form source and drain regions. The SiN_x film was removed and 50 nm thick SiN_x film was deposited again by sputtering method, followed by activation annealing at 1200 ^oC for 3 min. N ion implantation processes were adopted to fabricate isolation regions in GaN MISFETs [9]. The simulated impurity profiles of Si and N ions are shown in Fig. 2. Ohmic contact electrodes and gate electrodes were formed by depositing Ti/Al (50/300 nm) layers, followed by post metallization annealing at 550 ^oC for 1 min. Gate length, the spacing between the Si-ion-implanted regions in this case, was 2 μm and gate width was 100 μm.

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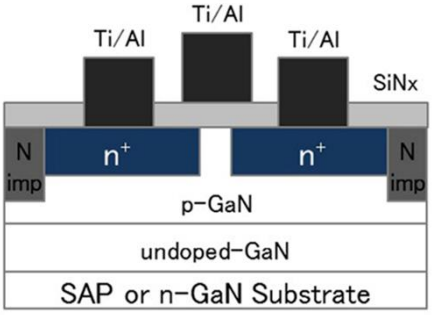


Fig. 1. Schematic cross section of the fabricated GaN MISFET.

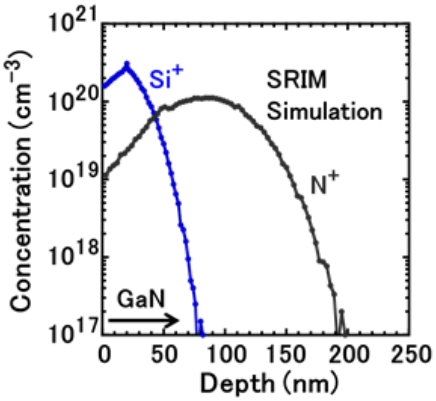


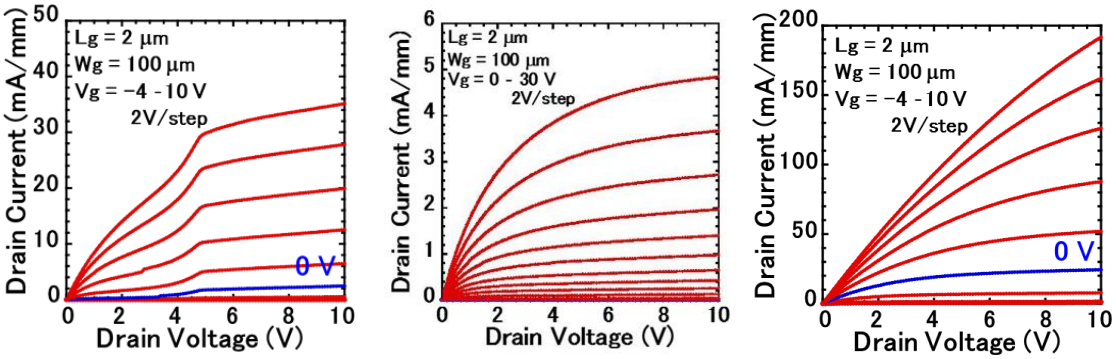
Fig. 2. Simulated impurity depth profiles of Si ion implanted into source/drain regions and N ion implanted into field isolation regions.

III. Results and discussion

Figures 3a-c show I_d-V_d characteristics of the GaN MISFETs using p-GaN (Mg : 0.5-1 × 10^{18} cm^{-3}) layers grown on sapphire and n-GaN substrates. From Figs. 3a and 3c, the MISFET exhibited normally-on characteristics. On the other hand, fine pinch-off characteristics were observed in entire measured range with little leakage current as shown in Fig. 3b. Figures 4a-c show I_d-V_g characteristics of the GaN MISFETs using p-GaN (Mg : 0.5-1 × 10^{18} cm^{-3}) layers grown on sapphire and n-GaN substrates. At V_d = 10 V, V_{th} of the MISFETs using p-GaN (Mg : 1 × 10^{18} cm^{-3}) layers on the sapphire and that on the n-GaN substrate obtained from extrapolation of linear portion of transconductance was about -2.5 V and 9 V, respectively. (Our determination of the V_{th} is more stringent than that by the conventional extrapolation of linear portion of I_d, because I_d vanishes at the newly defined V_{th}.) The latter V_{th} of 9 V was still smaller than theoretically calculated value of 11 V using the Mg concentration.

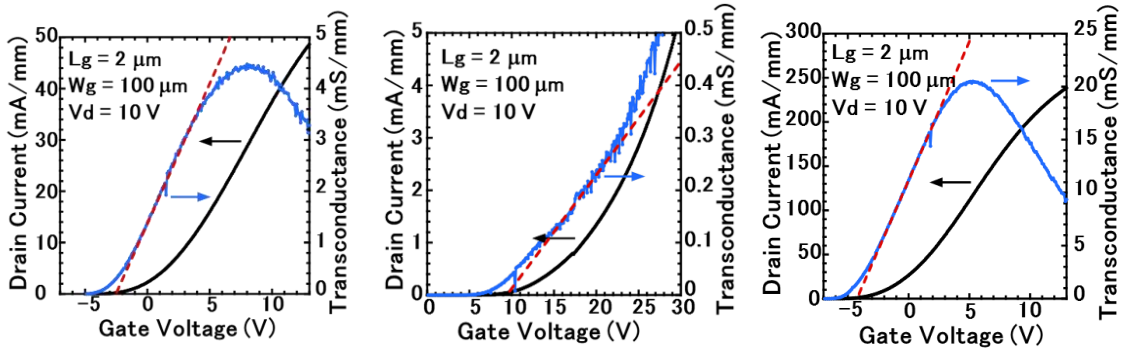
Table 1 shows measured V_{th} of the fabricated GaN MISFET in each condition and calculated V_{th} at $N_a - N_d = 5 \times 10^{17}$ cm^{-3}. The fabricated MISFETs using a p-GaN (Mg : 1 × 10^{18} cm^{-3}) layer grown on the n-GaN substrate was close to the calculated value using $N_a - N_d = 5 \times 10^{17}$ cm^{-3}. Therefore, donor-type defects such as N vacancies [10] were generated by the process damage, and one half of the doped Mg acceptors was compensated by the defects. The reason for the very low V_{th} of the MISFET on the sapphire was supposed that much more defects were generated in the GaN layer with high density dislocations.

Figure 5 shows V_{th} dependence with the gate length for MISFETs on sapphire and on n-GaN substrates. By our optimized ion-implantation process, V_{th} of the MISFETs on sapphire and n-GaN substrates were not dependent with the gate length. The MISFETs on the n-GaN substrate showed stably high V_{th} around 9 V by the high quality epitaxial layers on the freestanding GaN substrates.



(a) (b) (c)

Fig. 3. I_d-V_d characteristics of the fabricated GaN MISFETs on (a) sapphire (Mg : 1 × 10^{18} cm^{-3}) and (b) n-GaN substrate (Mg : 1 × 10^{18} cm^{-3}) and (c) n-GaN substrate (Mg : 5 × 10^{17} cm^{-3}).



(a) (b) (c)

Fig. 4. I_d-V_d characteristics of the fabricated GaN MISFETs on (a) sapphire (Mg : 1 × 10^{18} cm^{-3}) and (b) n-GaN substrate (Mg : 1 × 10^{18} cm^{-3}) and (c) n-GaN substrate (Mg : 5 × 10^{17} cm^{-3}).

Table 1. Measured V_{th} of the fabricated GaN MISFETs in each condition and calculated V_{th} using $N_a - N_d = 5 \times 10^{17}$ cm^{-3}.

Substrate	Mg concentration (cm^{-3})	V_{th} (V)
SAP	1 x 10^{18}	-2.5
n-GaN	1 x 10^{18}	9.0
n-GaN	5 x 10^{17}	-4.0
Calculated	N_a - N_d = 5 x 10^{17}	8.7

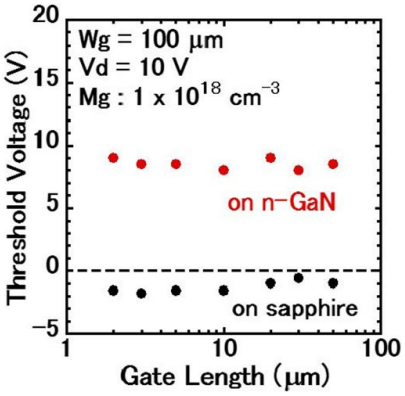


Fig. 5. V_{th} dependence on gate length for MISFETs on a sapphire and on a n-GaN substrate.

IV. Conclusions

We have demonstrated normally-off GaN MISFETs using a p-GaN (Mg : 1×10^{18} cm^{-3}) layer grown on free-standing GaN substrates. At V_d = 10 V, V_{th} obtained from extrapolation of linear portion of transconductance was about 9 V which was close to the calculated value using $N_a - N_d = 5 \times 10^{17}$ cm^{-3}. This result suggests that donor-type defects were generated by the process damage and partially compensated Mg acceptors. The MISFETs on the n-GaN substrate showed high V_{th} of about 9 V that does not have a dependence with the gate length. These excellent normally-off characteristics were brought by the low defect density GaN epitaxial layers and our optimized ion implantation process which minimizes the additional defect formation during high temperature annealing.

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