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DAMAGE-FREE FABRICATION OF HIGH BREAKDOWN VOLTAGE GaN p-n JUNCTION DIODES BY WET ETCHING PROCESS

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Pulsed photo-electrochemical (PEC) etching was performed to fabricate mesa-structure vertical GaN p-n junction diodes without process damages which were inevitable in conventional dry etching process. The damage-less etched surface was confirmed by photoluminescence and cathode luminescence measurements. The most beneficial property of the GaN p-n junction diodes by the PEC etching was much less variation in their breakdown voltages (3.83 - 3.88 kV) comparing with those by conventional dry etching (3.36 - 3.81 kV). These results indicate an excellent potential of the PEC etching in fabrication of GaN power devices.

I. Introduction

Recently the validity of GaN devices for power-conversion applications has been widely recognized because of supreme material properties of GaN and the related emerging researches have been conclusively reported.[1)] By the development and mass production of high quality freestanding GaN substrates,[2-4)] vertical structure GaN devices have been considered to be outstandingly efficient in those applications; hence, passionate research and development on the GaN power devices have been reported by many researchers.[5-24)] There have been several reports on vertical GaN p-n junction diodes[6,25,26)] with high breakdown voltage (V_B) up to 5 kV and low specific on-resistance (R_{on}) closing the limit of Baliga's figure of merit,[27)] which also proved the effectiveness of the vertical structure. A dry-etching process such as inductively coupled plasma-reactive ion etching (ICP-RIE) has been required for fabricating the vertical devices;[28,29)] however, damages to the GaN layers by high energy ions have been inevitable and degraded their performances.[7)] It was difficult to apply wet etching to GaN device processing because the etching simply has provided uncontrolled rough surface morphologies; however, continuous progress in photo-electrochemical (PEC) etching has revealed its abilities of damage-free wet etching on the GaN surface.[30-41)] Very recently, Horikiri et al. improved the PEC etching using high quality epitaxial layers grown on low dislocation density GaN substrates and clearly showed excellent deeply etched structures with smooth surfaces.[42,43)] Here we report fabrication of mesa-structure GaN p-n junction diodes using the PEC etching for the first time and show its impact on their current-voltage characteristics.

II. Experimental Methods

Epitaxial layers with the structure of p^+-GaN (Mg=2×10^{20} cm^{-3}, 30 nm)/p-GaN (Mg=1×10^{18} cm^{-3}, 500 nm)/un-GaN (Si<3×10^{15} cm^{-3}, 3.5 μm)/n^--GaN (Si=7×10^{15} cm^{-3}, 23 μm)/n-GaN (Si=2×10^{18} cm^{-3}, 2 μm) were grown by metal-organic vapor phase epitaxy

(MOVPE) on GaN substrates which were produced by void-assisted separation (VAS) method.[3-4] By simple 1-D Poisson's calculation, the reverse V_B of the p-n diode using this wafer was expected to be 3.9 kV assuming that the breakdown electric field of GaN was 3.0 MV/cm. Typical threading dislocation density of the substrate was as low as 1-3×10^6 cm^{-2} and the dislocations were uniformly spread out on the substrate, which was one of key requirements for obtaining uniform and smooth PEC etched surfaces.[42,43] Mesa-structure diodes with etched depth of approximately 1 μm were fabricated by the pulsed PEC etching or conventional ICP dry etching on adjacent areas of the same small chip (10×10 mm^2) for fair comparison. The structure of the diode is shown schematically in Fig. 1. A field-plate electrode was formed to reduce concentrations of electric field at the mesa edge.[5] The sizes of the Pd electrode and the mesa were 60 and 90 μm in diameter, respectively. PEC etching was performed by oxidizing GaN into Ga_2O_3 at the anode using an electrolytic solution of 0.01 M NaOH. Anode and cathode electrodes correspond to GaN-epi surface and Pt coil, respectively. The UV light source was Hg-Xe lamp with irradiation intensity of 9 mWcm^{-2} measured at 405 nm. The applied voltage was 1 V during PEC etching step. These conditions brought the etching rate of 25 nm/min. The detailed procedure of the PEC etching has been described in the previous reports.[42,43] A mask for wet etching was a spin-on-glass (SOG) layer with a thickness of 400 nm. The ICP dry etching was performed with Ar and CF_4 as etching gases under a low damage mode with an etching rate of 14 nm/min. The mask for the dry etching had a thick three-layer structure of SOG / SiO_2 / Ni (400/200/300 nm). Photoluminescence measurements were performed to the etched un-GaN surfaces at 77 K using focused He-Cd laser for excitation with a power of 3 mW. The etched surfaces were evaluated by a scanning electron microscope (SEM) Hitachi SU5000 with a cathode-luminescence (CL) function. Current-voltage (I-V) characteristics were evaluated using Agilent B1505A combined with an ultra-high-voltage unit at room temperature while measured chips were immersed in insulating oil.

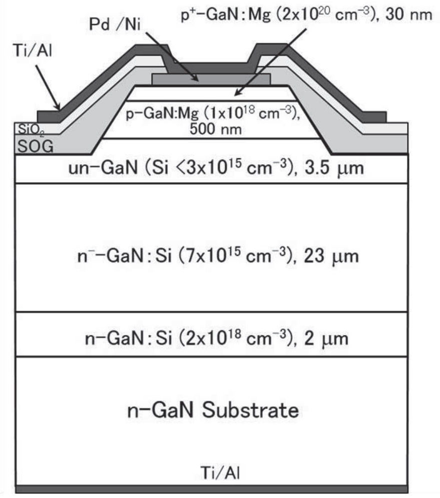

Fig. 1. Schematic cross section of the GaN p-n junction diode.

III. Results and Discussion

Figure 2 shows plan-view SEM images of the mesa structures formed by the PEC etching and the dry etching. The flat etched top of the exposed un-GaN was smooth for the both etching methods; however, the side wall by the PEC etching had much smoother surfaces than that by the dry etching. The jagged side walls by the dry etching were seemed to be caused by imperfect circular edge of the Ni

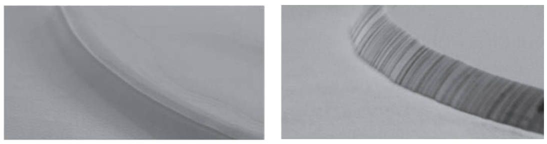

Fig. 2. SEM images of the mesa areas by the PEC etching (left) and the dry etching (right).

mask formed by a conventional lift-off process. Figure 3 shows PL spectra taken from the exposed un-GaN layers by the two etching methods. Sharp peaks at high energy side were near band-edge emission and its phonon replicas.[44] The PL intensity of these emissions from the dry-etched sample was lower than that from the PEC-etched sample by one order of magnitude, which indicated increase of non-radiative centers by the dry-etching damages. On the other hand, the PEC etching was damage-free, which was confirmed by the identical PL spectra taken from PEC-etched surface and as-grown surface of another n-GaN single epitaxial layer grown on the GaN substrate.

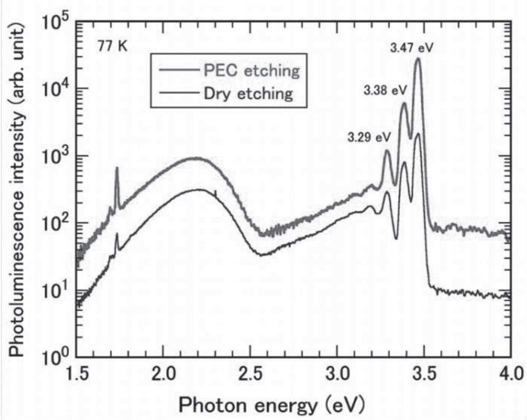

Fig. 3. (Color online) PL spectra taken from the exposed un-GaN layers by the PEC etching and the dry etching.

Plan-view CL images were taken with the mesa etched p-n junction wafer. Figure 4 shows the image taken at the area where the dry-etched multiple rectangular portion was surrounded by PEC-etched area. The sample was fabricated as the PEC-etched area was covered by a mask during the dry etching and vice versa. Several diodes were fabricated on each area. The dry-etched portion was apparently dark by the etching damages as the results of the PL spectra. Circular diodes showed dark images because the top p+-GaN/p-GaN layers had lower luminescence efficiencies than the un-GaN layer. Figure 5 shows the CL image of the mesa edge by the PEC etching. Many dark spots corresponded threading dislocations taking over from the substrate. Some spots were located at the mesa edge where a high electric field was concentrated under reverse biased conditions.

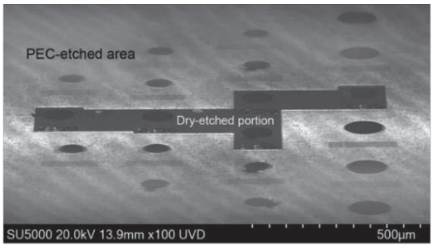

Fig. 4. CL image taken at the area where the dry-etched multiple rectangular portion surrounded by the PEC-etched area.

Figure 6 shows forward I-V characteristics of the diodes fabricated by the PEC etching and the dry etching. The current of the diode by the PEC etching governed by generation-recombination (n=2) then diffusion (n=1) transportations, which reflected the damage-free

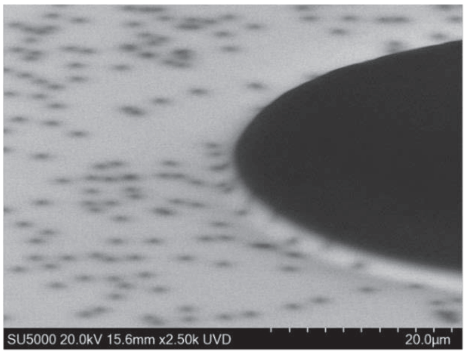

Fig. 5. CL image of the mesa edge by the PEC etching.

fabrication. The slightly higher Ron for the diodes by the PEC etching was due to a little side etching of the top p+-GaN layer because the SOG etching mask was partially peeled during the etching and the effective area of the anode contact was reduced. The peeling could be avoided by using a tougher mask such as Ti.[41,43] Figure 7 shows the reverse I-V characteristics of the diodes by the PEC etching and the dry etching. The diode by the PEC etching showed a higher V_B and lower leakage current. Figure 8 shows variations in the V_B of the diodes by the PEC and the dry etchings which were measured with six diodes for each etching method. (Some records were overlapped.) The diodes by the PEC etching showed higher breakdown voltages with smaller deviations (3.83 - 3.88 kV) compared with those (3.36 - 3.81 kV) by the dry etching. The highest V_B (3.88 kV) was close to the expected value by the 1-D Poisson's calculation. Every diode ended in a hard breakdown at the mesa edge; hence, the large variations in V_B for the diodes by the dry etching might be caused by the diversely damaged dislocations which lied on the jagged mesa side walls. On the other hand, the exposed dislocations on the side wall by the PEC etching as shown in Fig.5 were not seemed to fatally influence the V_B. The favorable impact and excellent potential of the PEC etching for fabricating GaN power devices were revealed by these examinations.

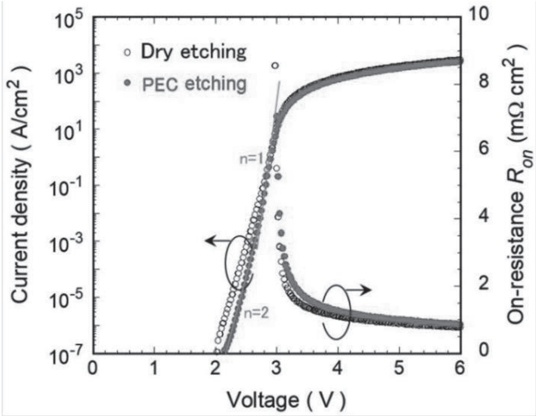

Fig. 6. Forward I-V characteristics of the diodes fabricated by the PEC etching and the dry etching.

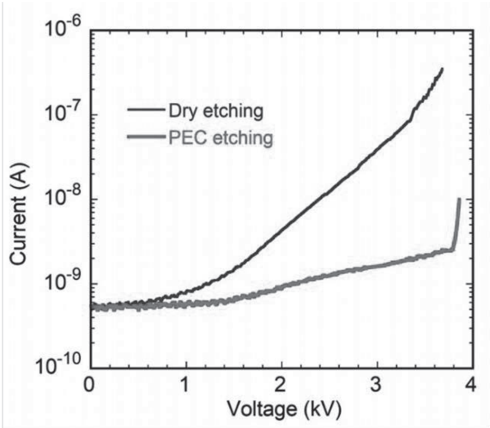

Fig. 7. Reverse I-V characteristics of the diodes fabricated by the PEC etching and the dry etching.

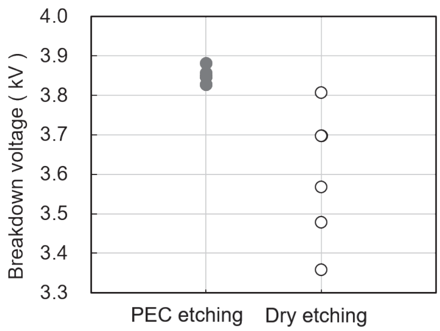

Fig. 8. Variations in the V_B of the diodes fabricated by the PEC etching and the dry etching.

IV. Conclusions

The PEC etching was applied for the first time to the fabrication of high breakdown voltage GaN p-n junction diodes with a fair comparison to the ICP dry etching. The free of damage to the GaN layers by the PEC etching were confirmed by PL and CL properties. The diodes by the two etching methods showed little difference in forward I-V characteristics; however, the V_B's of diodes by the PEC etching were improved with much less variations comparing with those by the dry etching. These results suggested that the damage-free PEC etching process would become an essential tool for high performance GaN power devices.

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