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A Network Model for Simulating a Semiconductor Device

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Abstract

The present paper describes a novel approach to modeling a semiconductor device based on a network model. The approach consists essentially of deriving a network, composed exclusively of fundamental circuit elements, such as resistors and current/voltage sources, directly from the governing equations of the device, then using this network model for analyzing the device's characteristics with the aid of a circuit simulator.

First, the method of derivation is outlined. Then, application of the full *drift-diffusion model* (DDM) *equivalent network* to a forward-biased p-n junction will be presented.

1 Introduction

Among the many conmputer aids to the design of intergrated circuits, it is no doubt that the universal circuit simulator SPICE [1] is the most widely used, not only at design sites in the industry, but also at every engineering school the world over. During the days prior to the advent ofVLSI (Very-Large-Scale Intergration), SPICE served not only as a circuit analyzer, but also as a simulater for electrial characteristics of various semiconductor device, using its built-in device models. however, as the design rule of intergrated circuits is scaled downed to the submicron size, it becomes difficult for these built-in models, including lately developed advanced MOS model [3], which essentially consist of a number of simple mathematical formulae, to cope with the various two-or three-dimenstional effects that turn conspicuous in these miniaturized devices. The only alternative is to rely on a rigorous numerical solution of basic governing equations of the device [2] in a two-dimensonal space, or even a three-dimensional space [4], if necessary. In this case, one has to develop a completely different and sophisticated computer aid, usually called a *device simulator*. Such device simulater is by far a complex piece of work that requires, for its successful realization, not only a thourough understanding of the physics of the device, but also the mathematics of numerical calculation as well as a high skill in the programming technique.

The network model described here is developed to fill the demand for such a rigorous numerical device model without the necessity of developing a dedicated device simulator. Starting from the very basic governing equations of a semiconductor device, we first show how to derive the

corresponding network model using the traditional finite element discretization. The network model is then expressed in the form of a conventional SPICE netlist on which a SPICE simulation is carried out to obtain information on device characteristics in terms of node voltages and/or branch currents of the network. For simplicity and without loosing generality, we will treat the two-dimensional DDM case, where the three basic governing equations are the Poisson and two continuity equations for electorns and holes, respectively.

As an example, we will apply our method to a forward-biased p-n junction where all three above mentioned equations must be solved simultaneously. The result obtained using the network model will be compared with a *dedicated* numerical device simulator.

2 Derivation of the network-model

2.1 Poisson equation

The integral form of Poisson equation in a two-dimentional space is given by Eq. (1).

$$\int_S \left(\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}\right) dS+\int_S \frac{q}{\varepsilon_r\varepsilon_0}(p-n+N_D-N_A)\,dS=0, \tag{1}$$

where ψ, S, ε_r, ε_0, q, N_A, N_D, p and n denote potential, a closed surface, specific dielectric constant of device material, permittivity of vacume, electronic charge, acceptor and donor densities, hole and electron densities, respectively. p and n are assumed to a obey Boltzmann distribution and thus given by Eqs. (2) and (3), respectively.

$$p=n_i\exp\left\{\frac{q(\phi_p-\psi)}{kT}\right\}, \tag{2}$$

$$n=n_i\exp\left\{\frac{q(\psi-\phi_n)}{kT}\right\}, \tag{3}$$

where n_i is intrinsic carrier density, k, Boltzmann constant, T, absolute temperature, ϕ_n and ϕ_p quasi-Fermi potentials for electron and hole, respectively.

Fig. 1 shows the magnified area around a node in a rectangular grid scheme used for discretizing the device under consideration. Applying Eq. (4) to the hatched control volume (CV), at the same time approximating it by a finite difference equation, one arrives at the following expression.

$$\begin{aligned}&(\psi_E-\psi_X)\cdot\sigma\frac{DMY_j}{DX_{i+1}}+(\psi_N-\psi_X)\cdot\sigma\frac{DMX_i}{DY_j}\\&(\psi_W-\psi_X)\cdot\sigma\frac{DMY_j}{DX_i}+(\psi_S-\psi_X)\cdot\sigma\frac{DMX_i}{DY_{j+1}}\\&+\sigma\frac{q}{\varepsilon_r\varepsilon_0}(p-n+N_D-N_A)\cdot DMX_i\cdot DMY_j=0\end{aligned} \tag{4}$$

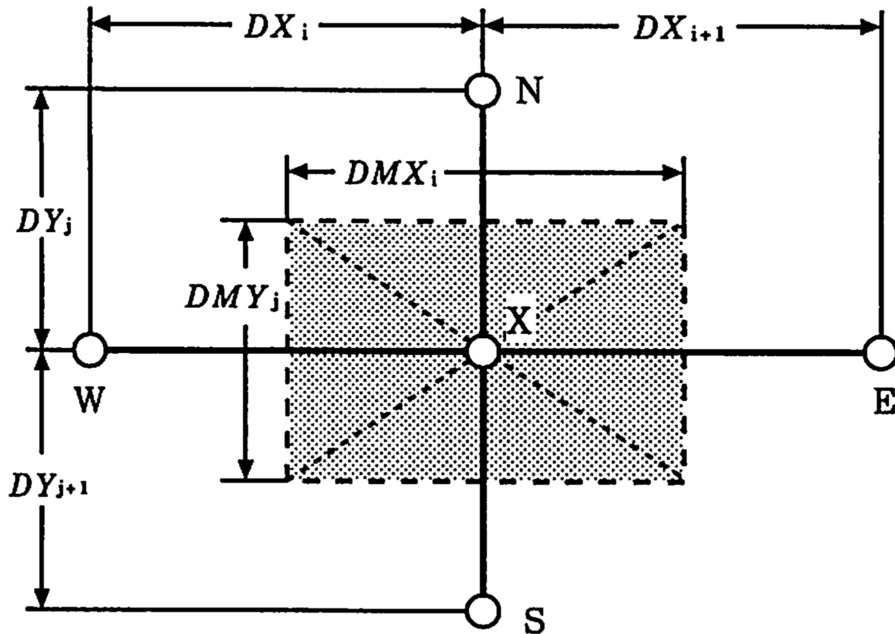

Fig. 1 Rectangular grid scheme for the finite difference discretization.

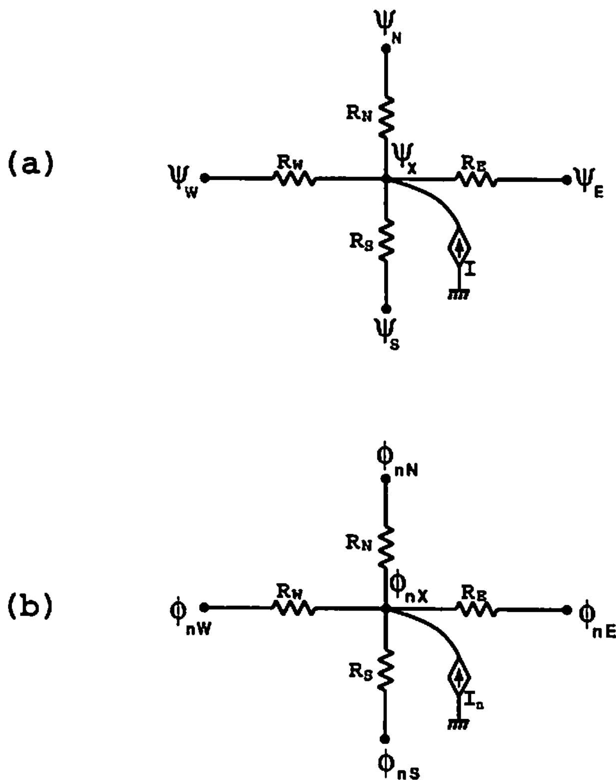

Fig. 2 Equivalent networks.
(a) for Poisson equation,
(b) for continuity equation for electrons.

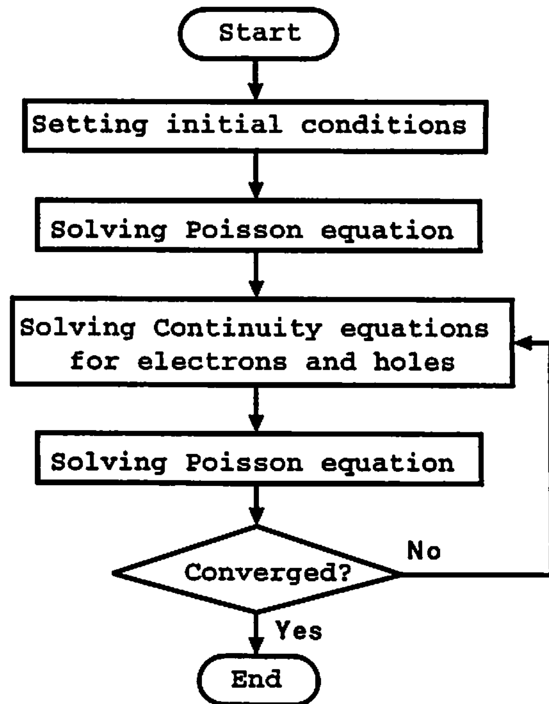

Fig. 3 Algorithm of simulation.

Note that σ, the conductivity of device material, has been intentionally multiplied to both side Eq. (4) to convert each of the equation into a current. In other words, Eq. (4) is but the Kirchhoff 's current law applied to node X. With this in mind, it is now possible to replace the hatched area in Fig. 1 by an equivalent circuit shown in Fig. 2 (a). The four resistors and the constant current source are given as follows.

$$R_E=\rho\frac{DX_{i+1}}{DMY_j\times 1},\quad R_N=\rho\frac{DY_j}{DMX_i\times 1}$$
$$R_W=\rho\frac{DX_i}{DMY_j\times 1},\quad R_S=\rho\frac{DY_{j+1}}{DMX_i\times 1} \tag{5}$$
$$I=\sigma\frac{q}{\varepsilon_0\varepsilon_r}(p-n+N_D-N_A)\cdot DMX_i\cdot DMY_j$$

Here $\rho=\sigma^{-1}$ is the material resistivity and 1 in the denominator of four expressions for resisitor values denotes the unit length in the direction into the surface of the paper. I is a current source dependent of potential ψ as well as quasi-potentials ϕ_n and ϕ_p by virtue of Eqs. (2) and (3).

2.2 Continuity equations

Continuity equations for electrons and holes are written as follows, using quasi-Fermi potentials as variables [2].

$$\mathrm{div}(\mu_n n\ \mathrm{grad}\phi_n)=0 \tag{6}$$
$$\mathrm{div}(-\mu_p p\ \mathrm{grad}\phi_p)=0 \tag{7}$$

Here μ_n and μ_p are electron and hole mobilities, ϕ_n and ϕ_p denote quasi-Fermi potentials for electrons and holes, respectivery. Note that generation and recombination have been neglected for simplicity.

If the above Eq. (6) is integrated over the control volume of Fig. 1, then the following expression results, provided that mobility μ_n is assumed constant for simplicity.

$$\mu_n\int_S\left[\frac{\partial^2\phi_n}{\partial x^2}+\frac{\partial^2\phi_n}{\partial y^2}+\frac{q}{kT}\left\{\frac{\partial\psi}{\partial x}\frac{\partial\phi_n}{\partial x}+\frac{\partial\psi}{\partial y}\frac{\partial\phi_n}{\partial y}-\left(\frac{\partial\phi_n}{\partial x}\right)^2-\left(\frac{\partial\phi_n}{\partial y}\right)^2\right\}\right]dS=0 \tag{8}$$

which, upon applying the same procedure as the case of Poisson equation, yields the following finite difference equation.

$$\begin{aligned}&(\phi_{nE}-\phi_{nX})\cdot\sigma\frac{DMY_j}{DX_{i+1}}+(\phi_{nE}-\phi_{nX})\cdot\sigma\frac{DMX_i}{DY_{j+1}}\\&+(\phi_{nW}-\phi_{nX})\cdot\sigma\frac{DMY_j}{DX_i}+(\phi_{nS}-\phi_{nX})\cdot\sigma\frac{DMX_i}{DY_j}\\&+(\psi_E-\psi_W)(\phi_{nE}-\phi_{nW})\cdot\sigma\frac{q}{4kT}\frac{DMY_j}{DMX_i}+(\psi_N-\psi_S)(\phi_{nS}-\phi_{nN})\cdot\sigma\frac{q}{4kT}\frac{DMX_i}{DMY_j}\\&-(\phi_{nE}-\phi_{nW})^2\cdot\sigma\frac{q}{4kT}\frac{DMY_j}{DMX_i}-(\phi_{nS}-\phi_{nN})\cdot\sigma\frac{q}{4kT}\frac{DMX_i}{DMY_j}=0\end{aligned} \tag{9}$$

This can be replaced again by an equivalent network as shown in Fig. 2 (b), where the four resistors and the current source are given as follows.

$$
\begin{aligned}
&R_{nE} = p\frac{DX_{i+1}}{DMY_j \times 1}, \quad R_{nN} = p\frac{DY_j}{DMX_i \times 1} \\
&R_{nW} = p\frac{DX_i}{DMY_j \times 1}, \quad R_{nS} = p\frac{DY_{j+1}}{DMX_i \times 1} \\
&I_n = (\psi_E - \psi_W)(\phi_{nE} - \phi_{nW}) \cdot \sigma \frac{q}{4kT}\frac{DMY_j \times 1}{DMX_i} \\
&\quad + (\psi_S - \psi_N)(\phi_{nS} - \phi_{nN}) \cdot \sigma \frac{q}{4kT}\frac{DMX_i \times 1}{DMY_j} \\
&\quad - (\phi_{nE} - \phi_{nW})^2 \cdot \sigma \frac{q}{4kT}\frac{DMY_j \times 1}{DMX_i} \\
&\quad - (\phi_{nS} - \phi_{nN})^2 \cdot \sigma \frac{q}{4kT}\frac{DMX_i \times 1}{DMY_j}
\end{aligned}
\tag{10}
$$

Subscript n stands for electron and, similar to the above case of Poisson, I_n is a controlled current source, dependent of both ψ and ϕ_n.

A similar finite difference expression and similar equivalent network for Eq. (7) can be obtained easily by virtue of duality, and therefore, is omitted here for brevity.

3 Calculation procedure

With the above-developed three networks for three variables, namely ψ, ϕ_n, and ϕ_p, we are now in the position to solve whatever device problem that is governed by the basic equations. The calculation involving three network associated with three basic equations, can be carried out either *en bloc*, i.e. collectively using a netlist corresponding to all three equations, or successively using three netlists for three equations one-by-one in an iterative manner to ensure self-consistency of the solution. Here, since we are using a PC-environment with limited memory availability, we selected the successive procedure, which is illustrated by the flow chart of Fig. 3. Note, as a matter of course, that in the case when only the Poison/Laplace equation is to be solved, the loop for continuity equations is bypassed without any iteration.

4 An example and results

In the following example, constant grid size for the lattice system of Fig. 1 will be assumed, for simplicity. In other words, we will always have

$$\cdots = DX_{i-1} = DX_i = DX_{i+1} = \cdots = DX,$$

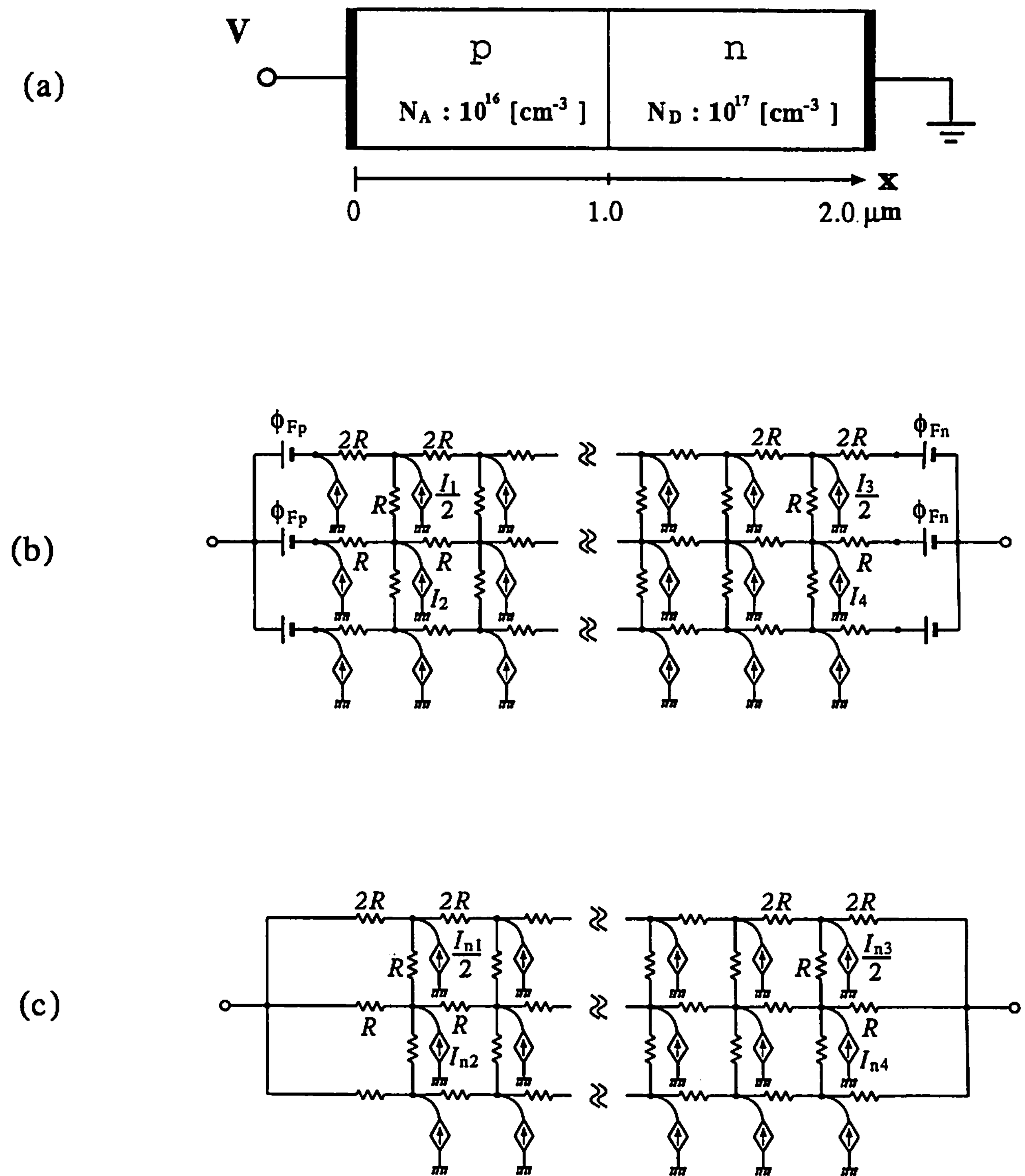

Fig. 4 A forward-biased p-n junction.

(a) the entire structure;

(b) equivalent network for Poisson equation;

(c) equivalent network for electron continuity equation.

$$\cdots = DY_{j-1} = DY_j = DY_{j+1} = \cdots = DY,$$
$$\cdots = DMX_{i-1} = DMX_i = DMX_{i+1} = \cdots = DMX = DX,$$
$$\cdots = DMY_{j-1} = DMY_j = DMY_{j+1} = \cdots = DMY = DY.$$

To show the simplicity and efficacity of the network model in simulating a semiconductor device, let us consider the case of a two-dimensional forward-biased p-n junction of the structure shown in Fig. 4 (a), with its equivalent Poissonnetwork and electron continuity network shown in Figs. 4 (b) and (c), respectively. The network for hole continuity equation is similar to the one for electron and, therefore, not shown for brevity. Dirichlet boundary condition is applied to electrodes, and Neumann boundary condition to side walls of the structure.

Figures 5 and 6 show the results obtained by the present method (◇ ◇ ◇ ψ (c), ● ● ● ϕ_n (c) and ○ ○ ○ ϕ_p (c)) together with those based on the conventional DDM device simulator (— ψ (d), ··· ϕ_n (d) and -- ϕ_p (d)) for two applied voltages of 0.1 V and −0.5 V, respectively. Strictly speaking only Fig. 5 corresponds to a forward bias. Fig. 6, corresponding to a reverse bias condition, is included for completeness. It is clear that the results based on the present approach are in excellent agreement with the conventional DDM device simulation approach. Fig. 7 shows the carrier distributions (for electrons and holes) within the p-n junction for the forward bias case. Needless tu say that result also agrees excellently with the DDM device simulator.

We should mention in passing that we still face a convergence problem as we increase the forward bias beyond 0.1 V. This, however, is not of primary importance and it may have something to do with the SPICE simulator itself. This matter is being investigated currently.

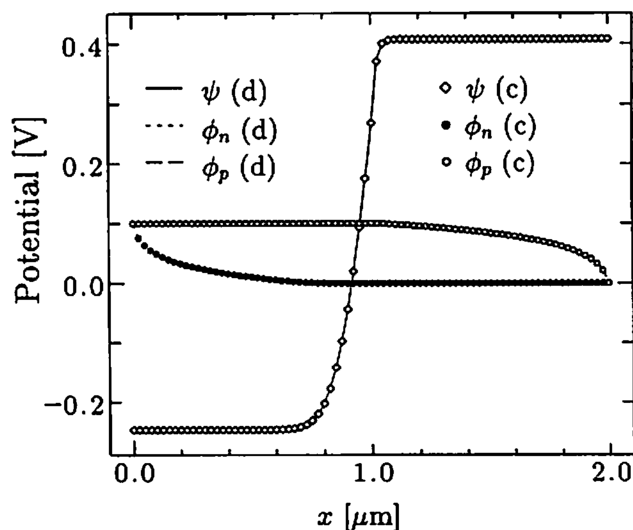

Fig. 5 Potential distribution inside the p-n junction corresponding to a forward-bias condition. Discrete points ◇ ◇ ◇ ψ (c), ● ● ● ϕ_n (c) and ○ ○ ○ ϕ_p (c) are results based on the network model, while continuous curves — ψ (d) , ··· ϕ_n (d) and -- ϕ_p (d) are obtained using a *dedicated* numerical DDM device simulator.

5 Conclusion

We have presented a new approach to modeling a semiconductor/conductor device using a network composed exclusively of simple and basic circuit elements directly derived from the very governing equations of the device, namely Poisson equation and continuity equations for electrons and holes,

respectivery. The network model's simplicity and efficacity have been proved through a typical example of a forward-biased p-n junction where all three basic semiconductor equations are solved simultaneously. The result obtained with our approach is in excellent agreement with a conventional *dedicated* numerical DDM simulator.

Our approach, therefore, can serve as a substitute for an otherwise labor-and time-consuming work of developing a *dedicated* device simulator.

The present paper has treated only the steady-state operation of the device under consideration. Our approach, however, lends itself readily to treating the time-varying problem, provided some suitable modification be made to the equivalent networks of Figs. 2 (a) and (b). This will constitute the subject of our next work to be reported in the future.

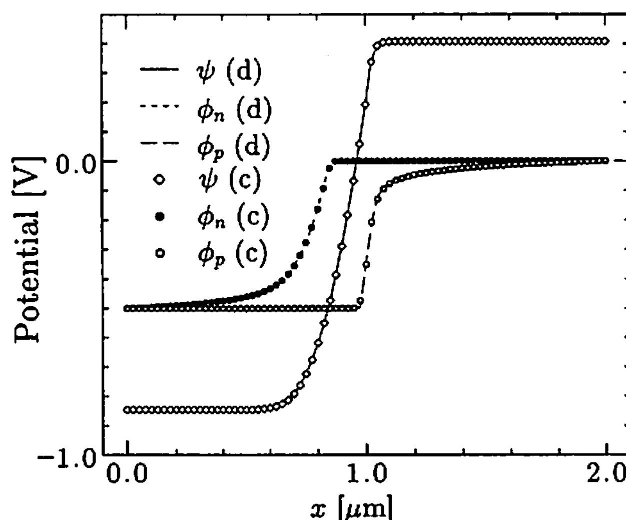

Fig. 6 Potential distribution inside the p-n junction corresponding to a reverse-bias condition. Notations and symbols are identical with those of Fig. 5.

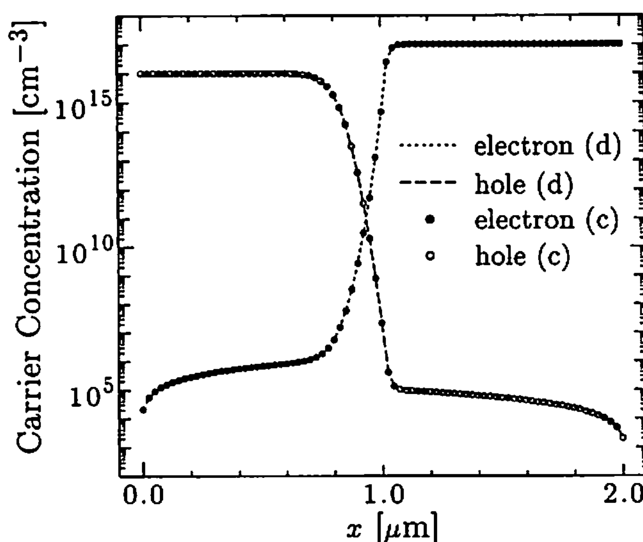

Fig. 7 Carrier distribution inside the p-n junction. Discrete points ●●● and ○○○ are results based on the present network model, while continuous curves ···· and --- are those obtained by the *dedicated* numerical DDM device simulator.

Acknowledgement

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